

Serial No. 09/479708

2815
#16 / IDS
10-2-03
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IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Inventor(s): Allen Paine Mills Jr.
Case: 11
Serial No.: 09/479708
Filing Date: January 7, 2000
Examiner: M.E. Warren Group Art Unit: 2815
Title: Method And Apparatus For Temperature Compensation Of Read-Only Memory

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SIR:

INFORMATION DISCLOSURE STATEMENT
PETITION AND CERTIFICATION UNDER 37 CFR 1.97(e)(1)

The Commissioner is hereby petitioned to consider the enclosed Information Disclosure Statement.

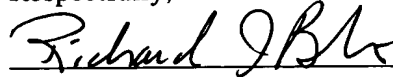
In accordance with 37 CFR 1.97(e)(1), the enclosed Information Disclosure Statement, with attached reference(s), is submitted for consideration in the above-identified application.

I certify that each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement. Copies of the listed documents are enclosed together with the search report that listed these documents.

A translation of FR 2 071 501 A is not provided. The reference is identified as technological background. As required by 37 C.F.R. § 1.97(a)(3), a concise explanation of the relevance of this reference is provided.

In the event of any non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit Agere Systems Deposit Account No. 50-1735 as required to correct the error.

Respectfully,



Richard J. Botos, Attorney

Reg. No. 32,016

610-712-8520

Date: September 10, 2003

Docket Administrator

Agere Systems Inc.

4 Connell Drive, Room 4U-533C

Berkeley Heights, NJ 07922-2747

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Asst. Commissioner of Patents and Trademarks,
Washington, D.C. 20231, on Sept. 10, 2003


Date

Concise Explanation of Relevance Pursuant to 37 C.F.R. § 1.97(a)(3).

FR 2 071 501 A

The reference, cited as technological background, describes a memory matrix that has linear resistors (35). The resistors cross the lines (31) and columns (32) of the memory.

